Multiresolution Image Sensor

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***Abstract*— The recent development of the CMOS active pixel sensor (APS) has, for the first time, permitted large scale integration of supporting circuitry and smart camera functions on the same chip as a high-performance image sensor. This paper reports on the demonstration of a new 128 × 128 CMOS APS with programmable multiresolution readout capability. By placing signal processing circuitry on the imaging focal plane, the image sensor can output data at varying resolutions which can decrease the computational load of downstream image processing. For instance, software intensive image pyramid reconstruction can be eliminated. The circuit uses a passive switched capacitor network to average arbitrarily large neighborhoods of pixels which can then be read out at any user-defined resolution by configuring a set of digital shift registers. The full resolution frame rate is 30 Hz with higher rates for all other image resolutions. The sensor achieved 80 dB of dynamic range while dissipating only 5 mW of power. Circuit error was less than −34 dB and introduced no objectionable fixed pattern noise or other artifacts into the image.**

***Index Terms*— Focal plane array, image processing, imager, multimedia, sensor.**

I. Introduction

FOR a variety of image processing tasks, such as biological vision modeling, stereo range finding, pattern recognition, target tracking, and transmission of compressed images, it is desirable to have image data available at varying resolutions to increase processing speed and efficiency. The user can then obtain a frame of data at the lowest resolution necessary for the task at hand and eliminate unnecessary processing steps. The multiresolution image data is usually generated through an image pyramid approach (implemented in software), and has been used extensively in recent years [1]–[4]. Typically, each image level is a low-pass filtered and down-sampled version of the prior level, although block averaging and down sampling can also be used to generate the pyramid [5]. In software, construction of the multiresolution pyramid is often the most computationally intensive and time consuming portion of the image processing task. For applications where power consumption is of concern, the power consumed by the processor while performing this task can be critical. These problems become especially severe for image processing tasks performed on large format imagers (e.g., 1024 × 1024) that are read out at video rates (30 frames/s).

CMOS active pixel sensor (APS) technology allows the integration of support electronics and smart camera functions onto the same chip as a high-performance image sensor [6]. The integration of support electronics such as timing and control, correlated double sampling, and analog to digital conversion leads to fewer components, thus increasing system robustness while reducing system mass and cost. The implementation of programmable multiresolution readout allows unprecedented camera functionality which eases the performance requirements of downstream image processing. The CMOS APS technology also enjoys other advantages over its charge-coupled device (CCD) counterpart such as ultra low power performance (50–100× lower than comparable CCD systems) and increased radiation hardness [7]. CMOS APS architectures [Fig. 1(a)] allow x–y addressability of the array for windows of interest and sparse sampling readout of the array. Unfortunately, sparse sampling the array, for example, by reading out every fourth pixel of every fourth row, reduces the amount of image data by a factor of 1/16 but introduces aliasing into the image. In the multiresolution sensor, regions of the array are averaged together (block or kernel averaging) and read out [Fig. 1(b)], leading to data reduction without aliasing effects.

The multiresolution CMOS APS is a 128 × 128 photogate array that is programmable to read out any size $n \times n$ block of pixels (kernel). Each kernel value represents the average of all the pixel values in its region. Averaging is done in the column readout circuitry so that the average value is based on a full resolution image. Combining the sensor's X–Y addressability with programmable resolution, the device can achieve true electronic zoom capability. In a standard digital camera, electronic zoom is achieved by mapping each pixel in a small area of interest to several display pixels. In contrast, the multiresolution sensor allows one to read out a small area of interest at a higher resolution than the full frame such that each pixel may be mapped to an individual display pixel much like an optical zoom lens allows one to capture more detail in a small area. This capability can also be used to increase processing speed of tracking algorithms where course resolution image data can be quickly read out and processed to determine an area of interest followed by read out of the area of interest at a higher resolution in the subsequent frame as illustrated in Fig. 2.

Details of the multiresolution sensor operation are discussed in Section II. Section III presents the test results from the fab-

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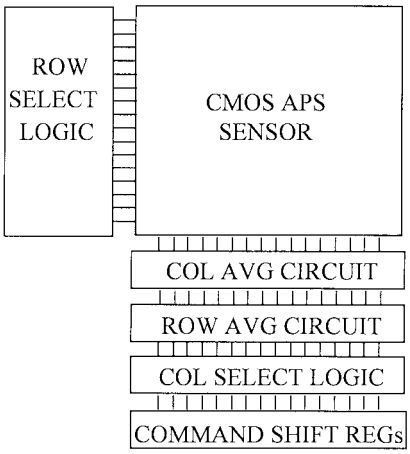
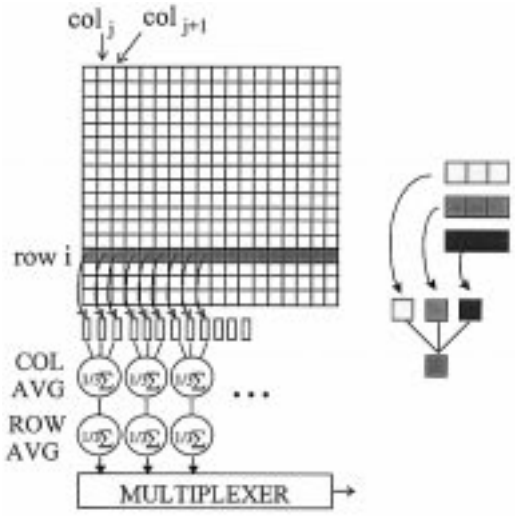


(a)



(b)

Fig. 1. (a) Programmable multiresolution CMOS active pixel sensor architecture and (b) example of column's functional configuration for 3 × 3 block averaging. (Actual neighborhood size is programmable.)

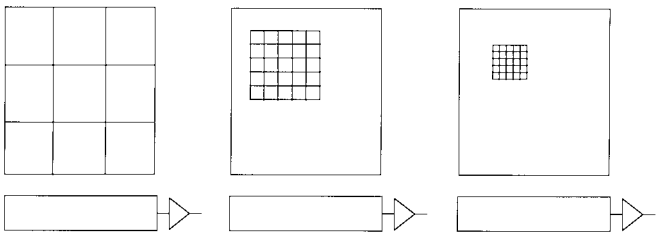


Fig. 2. Sensor X-Y addressability and multiresolution readout allows the user to zoom into an area of interest with increased resolution.

ricated chip. Finally, applications of the sensor are discussed in Section IV.

II. Design and Operation

A. Design Overview

The sensor contains a 128 × 128 photogate pixel array similar to previous APS arrays demonstrated at the Jet Propulsion Laboratory (JPL) [6]–[10]. At the bottom of each column in the array is a network of capacitors to store pixel reset and signal levels. The column circuitry also contains an additional capacitor and a set of switches to the adjacent column to perform averaging on any size square array of pixels called a kernel (rectangular kernels are also possible). Resolution of the sensor is set by the size of the kernel. Large kernels sizes are set for low resolution imaging requirements. The X–Y addressability of the sensor allows the user to zoom into areas of interest.

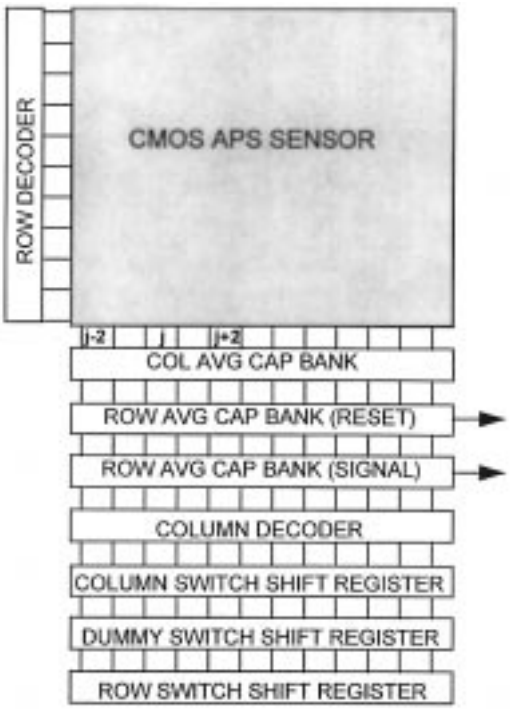


Fig. 3. Multiresolution image sensor block diagram.

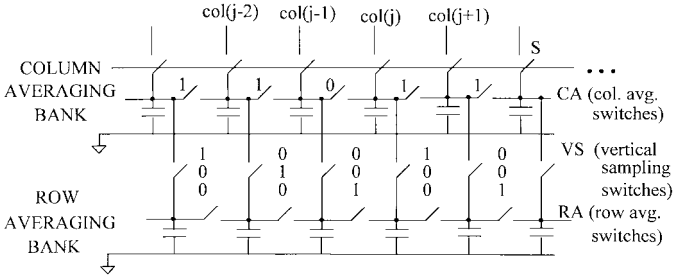


Fig. 4. Ideal switch and capacitor model for six columns configured for 3 × 3 block averaging.

Fig. 3 shows a block diagram of the sensor. A decoder at the side of the array selects a row of pixels for readout. Each pixel is controlled by a photogate signal enabling readout of integrated charge, a reset signal, and select signal to enable the buffered pixel data to drive the column output line. Column parallel circuitry at the bottom of the array samples the addressed row of pixel data simultaneously. The kernel size determines how a set of shift registers in the column circuits are configured. These shift registers control how the columns containing stored readout data are averaged and where the averaged row data is stored for subsequent

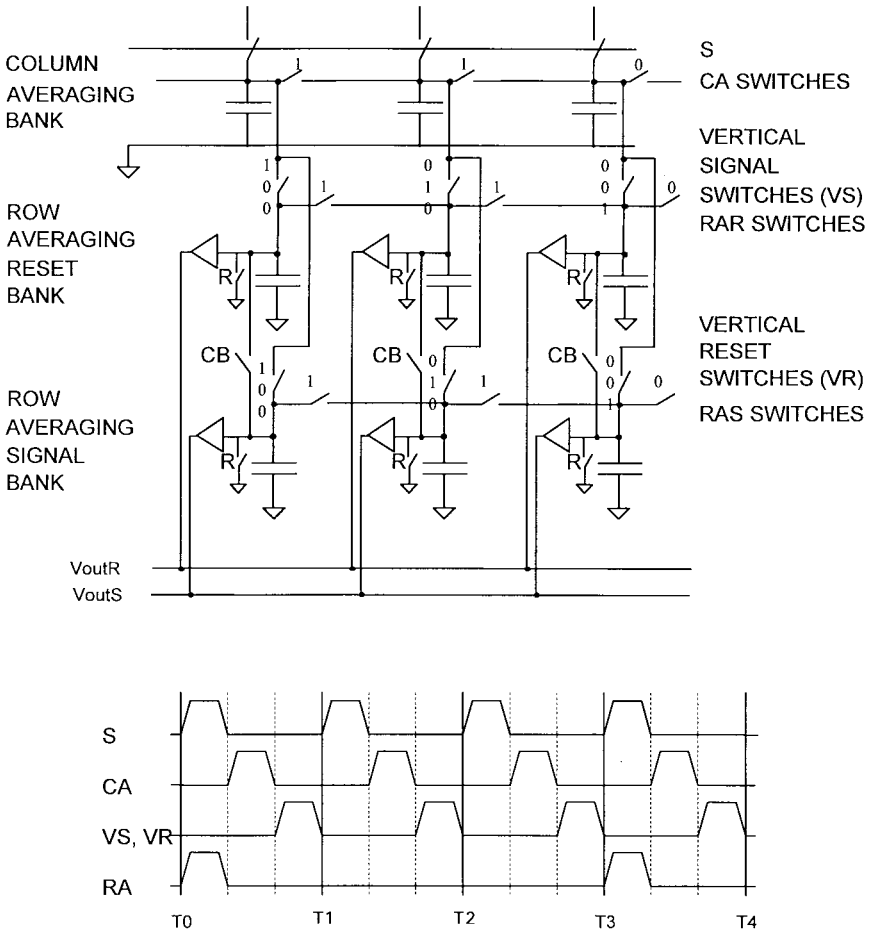


Fig. 5. Multiresolution column processing circuitry for three columns.

processing. A second decoder at the bottom of the array controls which columns containing the processed data are read out. The sensor's differential output circuitry performs correlated double sampling (CDS) to suppress pixel kTC noise, $1/f$ noise, and fixed pattern noise.

Row pixel data is read onto a column averaging capacitor with switches to its neighboring columns that are subsequently enabled resulting in averaged column data for that row (Fig. 4). Averaged column data for that row is stored on a second bank of capacitors in one of the columns of the kernel. Data from successively read out rows is stored in each of the remaining columns in the kernel. Shift registers in the readout circuitry are configured according to kernel size to determine which switches are enabled to perform averaging and where the averaged column data is stored.

Once all n rows of the kernel are read, they are averaged by connecting the second bank of capacitors together and mixing the charge. A shift register configured to enable dummy switches to correct for switch feedthrough effects is also included. Both reset and signal levels are processed for a kernel so that correlated double sampling and double-delta sampling operations can be performed.

Operation will be illustrated by stepping through the sequence for 3 × 3 block (kernel) averaging (Fig. 4). In this case, every third column average (CA) switch is open (i.e., deselected, denoted by bit 0 over the switch), while the other switches are closed (i.e., selected, denoted by bit 1 over the switch). Pixel signals are sampled onto the column averaging capacitors by globally pulsing (closing) the signal select switches (S). Charge redistributes such that the voltage on each capacitor in each block of three capacitors V_{i_ker} is the same such that

$$V_{i\_ker} = \frac{1}{n}\sum_{k=1}^{n} V_{j-k}$$

where n is the horizontal size (number of columns) of the block average (kernel), V_{j-k} the pixel voltage value of the (j–k)th column, and V_{i_ker} is the average value for the ith row in the kernel. These kernel row averages are then sampled onto the first capacitor in the n-capacitor block of the row averaging bank of capacitors. Column averaging is repeated with the next pixel row $(i+1)$ and these new $V_{(i+1)\_ker}$ kernel averages are sampled onto the second capacitor in the n-capacitor blocks of the row averaging bank of capacitors. The process is repeated until all n rows have been processed and n samples have been collected in n adjacent capacitors in the row averaging bank. The temporal switching sequence (digital pattern) is shown for the 3 × 3 kernel case (Fig. 5). After the n-samples $(V_i, V_{i+1}, \cdots, V_{i+(n-1)})$ have been collected, charge is redistributed by pulsing the row averaging (RA)

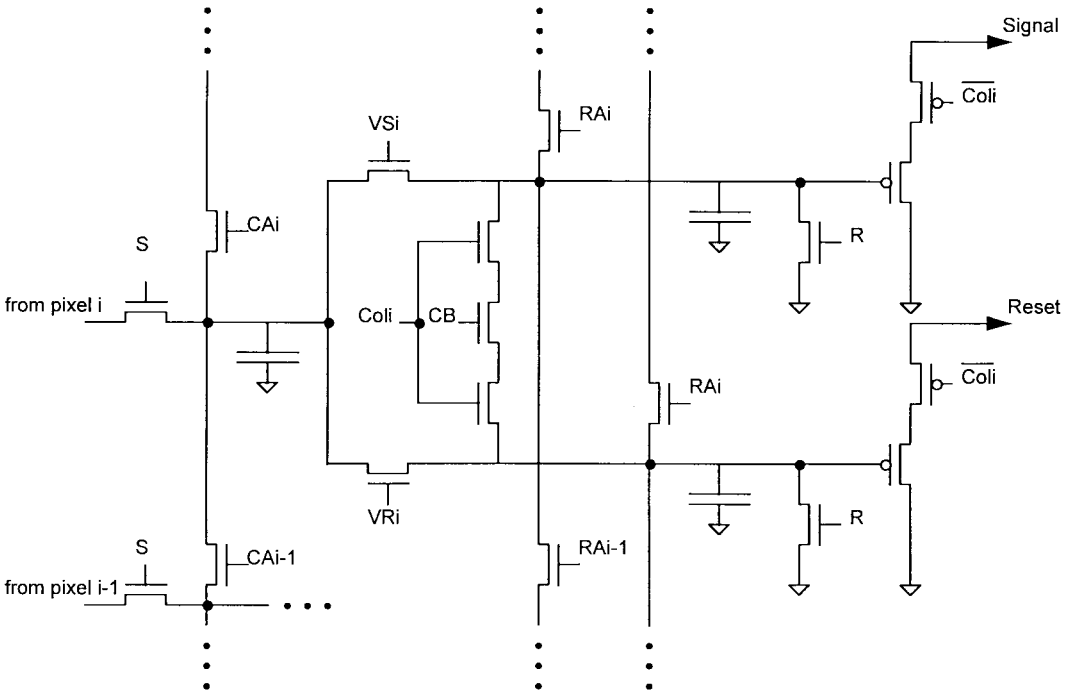


Fig. 6. Transistor-level schematic of column circuit. Capacitors are poly-diffusion linear capacitors.

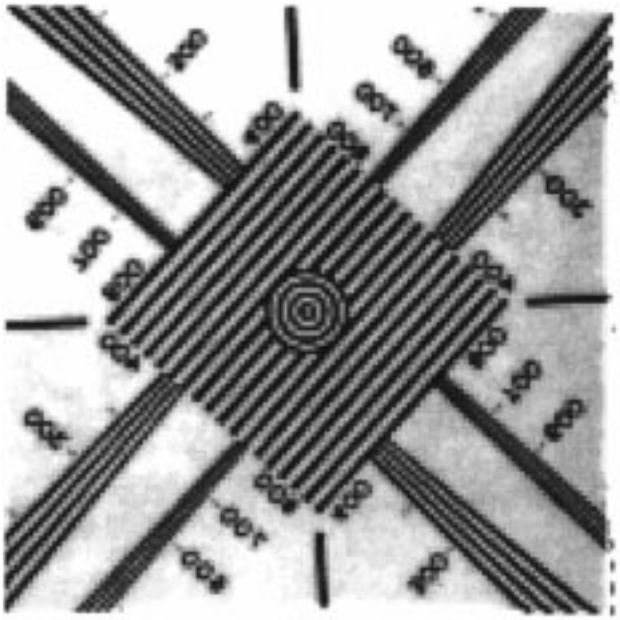
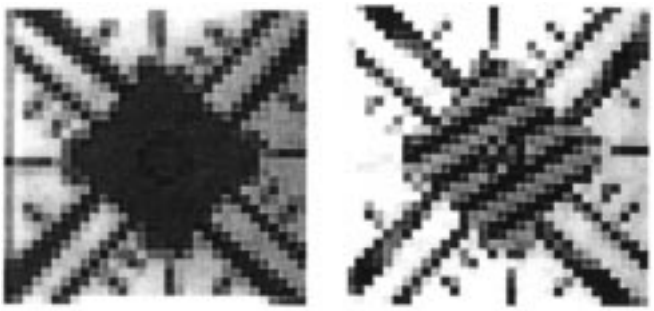


Fig. 7. Sensor's full resolution image (128 × 128).



(a) (b)

Fig. 8. (a) 4 × 4 block averaged time and (b) 1/4 subsampled image (no averaging).

switches with the same pattern used for the column averaging switches, resulting in the final block average

$$V_{ker} = \tfrac{1}{2} \sum_{i=1}^{m} V_{i\text{-}ker}$$

where m is the vertical size (number of rows) in the kernel. The constant factor of 1/2 arises from charge sharing between the column and row averaging capacitors when the column average is sampled onto the row averaging capacitor. Thus, for the first 3 × 3 kernel

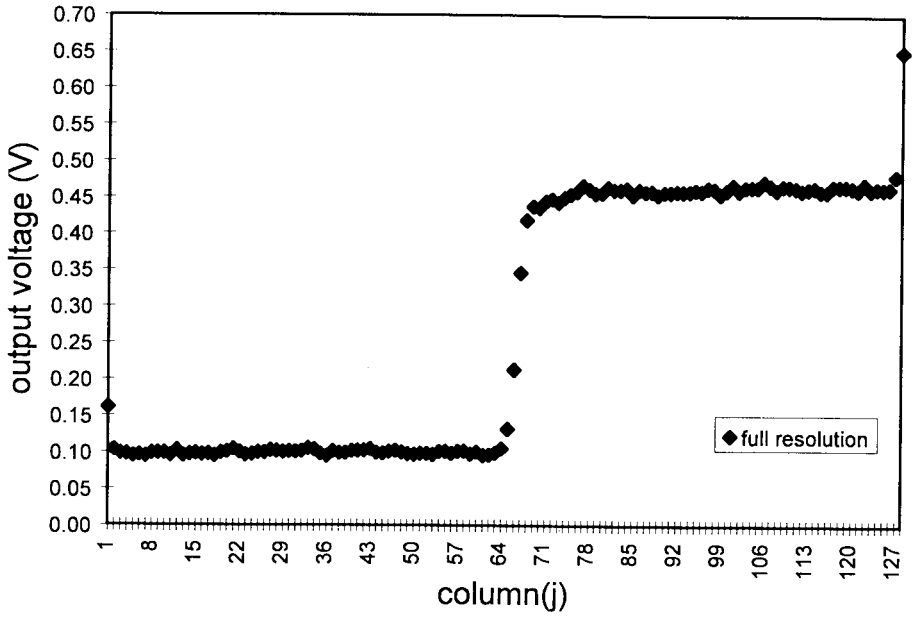
$$\begin{aligned} V_{ker\,0} = 1/2\{1/3[1/3(&V_{0,0} + V_{0,1} + V_{0,2}) \\ &+ 1/3(V_{1,0} + V_{1,1} + V_{1,2}) \\ &+ 1/3(V_{2,0} + V_{2,1} + V_{2,2})]\}. \end{aligned}$$

These kernel values are then scanned out of the array by reading out every nth capacitor in the row average bank. The row averaging capacitors are then reset (circuitry not shown) and the process is repeated to generate the next row of kernels.

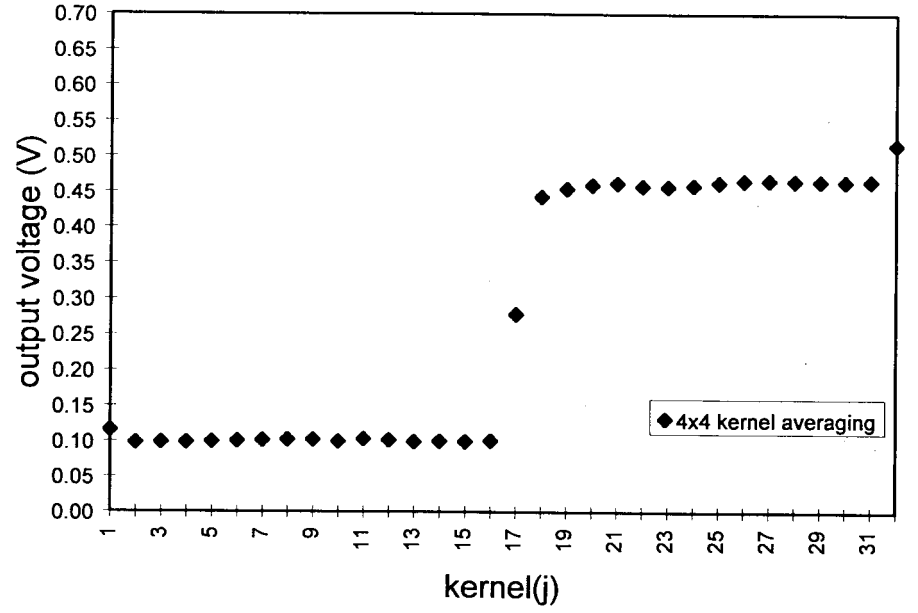
Note that in the configuration described above, kernels must be either square or rectangular, where the number of rows must be less than or equal to the number of columns.

B. Column Processing Circuitry

Shown in Fig. 5 is the actual column parallel circuitry for three columns. There is one bank of column averaging capacitors and two banks of row averaging capacitors (rather



(a)



(b)

Fig. 9. (a) Full resolution sensor output for one row of pixels and (b) 4 × 4 kernel output from sample image.

than the single bank shown in Fig. 4). One bank stores the row average pixel reset levels, and the other stores the row average pixel signal levels in order to perform on-chip double correlated sampling. The column averaging bank is used sequentially to horizontally average together the kernel row reset levels followed by the signal levels. The kernel reset switch to ground is shown as well as the column buffer amplifier for generating $V_{out}R$ and $V_{out}S$. The buffer amplifier is only enabled when the column is selected for readout.

The digital patterns shown are an example of the timing for a 3 × 3 kernel. They are generated by gating the output of the configuration shift registers and the timing signals shown in Fig. 5. The global timing signals are CA (enable column averaging), RA (enable row averaging), VS (sample signal onto row averaging capacitor), and VR (sample reset onto row averaging capacitor). Each of these global signals is gated with the output of one of the two configuration shift registers. The CA and RA signal are gated with the output of the same shift register (CARA shift register). The VS and VR signals are gated with the output of the second shift register (VSVR shift register).

The transistor-level schematic of the column circuit is shown in Fig. 6. The signals CA_i, RA_i, VS_i, and VR_i are the outputs from the corresponding global signals gated with the shift register output bit for that column. The buffer amplifier is a p-channel source follower. The CB signal is part of the double delta sampling readout scheme as reported in [9] used to reduce column fixed-pattern noise.

TABLE I
SENSOR CHARACTERISTICS

Array Size	128x128
Pixel Size	24 μm
Technology	1.2 μm n-well CMOS (HP)
Saturation level Vsat	1200 mV
Conversion gain	8 μV/e⁻
Read Noise (full resolution)	116 μV rms (15 e⁻ rms)
Dynamic Range	80 dB
Power@30Hz frame rate Vdd=5V, Vsat = 1200mV	5 mW
Vdd=4V, Vsat = 500mV	1.25 mW
Fixed Pattern Noise	3 mV p-p (0.25% of saturation)
Kernel averaging error	≤ 2 %

III. EXPERIMENTAL RESULTS

The sensor was fabricated through MOSIS in the HP 1.2-μm n-well CMOS process. The 128 $\times$ 128 photogate sensor has a pixel pitch of 24 μm. The total chip size is 4.8 $\times$ 6.6 mm. Table I lists some of the sensor characteristics for full resolution operation.

Fig. 7 shows a full resolution image of a test pattern used to demonstrate the sensor's block averaging. Fig. 8(b) shows the same image for the sensor operating in a subsampling mode where every fourth column of every fourth row is read with no averaging. Because the test target contains relatively high spatial frequency patterns, the subsampled image produces dramatic aliasing. Comparing this 32 $\times$ 32 image with the full resolution 128 $\times$ 128 image shows the appearance of both fewer stripes and diagonal stripes rather than parallel stripes relative to the edge of the square. The 32 $\times$ 32 image with 4 $\times$ 4 kernel averaging [Fig. 8(a)] reduces this effect because the pixel array is read at full resolution and subsequently averaged.

To measure how well the multiresolution sensor performs averaging, a test pattern containing a black and white stripe was imaged. The black–white edge (defocused) was positioned so that half the pixels in the kernels on the edge are black. Thus, the sensor output of the kernels aligned on top of the edge ideally should equal one-half of the difference between the totally white and black pixels. To measure the individual pixels in the kernel, subsampled data was first measured. Based on this subsampled raw image data, block averages were calculated for the pattern. This data was compared to the multiresolution sensor's output at different kernel sizes.

An example of the sensor's output for one of the rows is shown in Fig. 9 where the sensor's full resolution row data and 4 $\times$ 4 kernel output data are shown. The row shown [Fig. 9(a)] is one of four rows used to calculate the average from the full resolution image for comparison with the on-chip 4 $\times$ 4 kernel average. Fig. 9(b) illustrates the 4 $\times$ 4 kernel producing an output voltage at the average value of the four pixels at the black–white stripe edge (pixels in columns 65–68). Image data for 2 $\times$ 2, 4 $\times$ 4, and 8 $\times$ 8 kernel sizes were acquired for this test pattern. Analysis of kernel data for the entire frame versus the off-chip block average data based on full resolution data shows that the sensor is accurate to within 2% ($-$35 dB) of the ideal average value. The use of dummy switches for switch feedthrough compensation did not have a significant effect of the averaging accuracy.

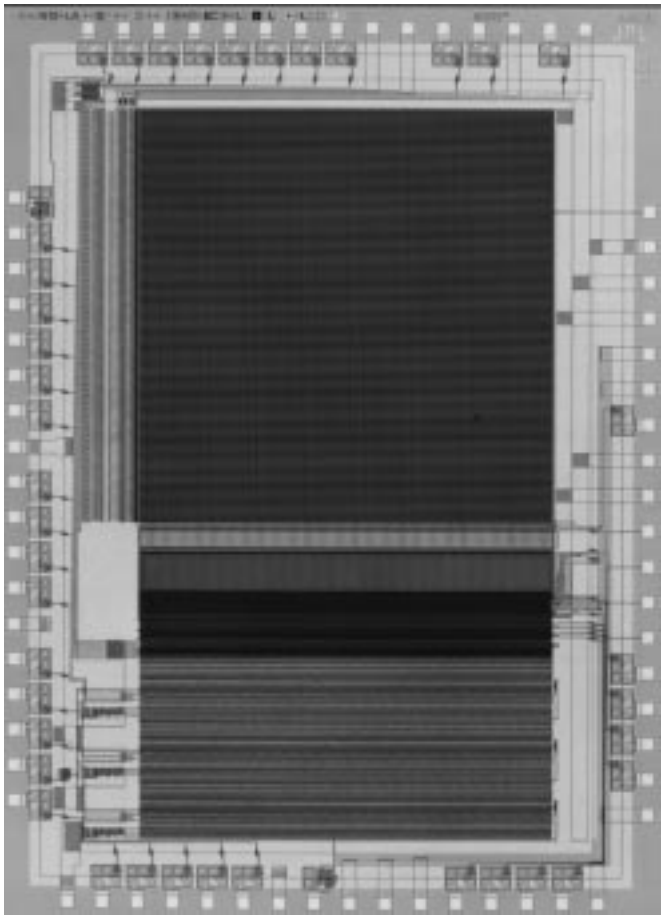


Fig. 10. Photograph of completed programmable multiresolution APS (128 $\times$ 128 array) IC.

Table I lists the results from sensor characterization tests similar to those described in [9]. The sensor exhibited very low fixed pattern noise and dissipated very little power. Overhead for performing on-chip block averaging is a small percentage of the sensor readout time and total power consumption. For lower resolutions, the frame rate increase above 30 Hz is approximately proportional to the number of pixels, $n \times n$, in the kernel.

IV. APPLICATIONS

Multiresolution readout capability is useful in a wide variety of imaging applications where real world systems impose constraints on format choices, processing speed, and bandwidth. A few applications that greatly benefit from such capability are described below.

Data Reduction: In many imaging applications today, bandwidth limitations impose severe constraints on the manipulation and transmission of image data. From computer telephony to internet Vmail, transmission of image data is becoming increasingly common. Tremendous amounts of compression are needed to realize these functions (e.g., a compression ratio of 320 : 1 is required to transmit a video graphics adaptor (VGA) 640 $\times$ 480-resolution image across a 28.8-kb/s phone line at video rates). Even without transmission, interfac-

(a) (b) (c) (d)

Fig. 11. Programmable multiresolution sensor output for (a) full resolution, (b) 2 × 2 kernel, (c) 4 × 4 kernel, and (d) 8 × 8 kernel configurations.

ing standard electronic cameras to a PC poses a compression challenge (e.g., 500 kbytes to 2 Mbytes per second enhanced parallel port (EPP), 12 MB for universal serial bus (USB) interface). One approach to achieving such compression is to reduce the amount of data being transmitted or compressed. In current CCD-based systems, such image editing may be realized by either throwing away image data (e.g., transmit the center of the image) or through image pyramid reconstruction. Unfortunately in the latter case, the required decimation and low-pass filtering is usually implemented in software, located beyond the bandwidth limited transmission link. Alternatively, memory and specialized hardware (digital signal processing (DSP) or custom application-specific integrated circuit (ASIC) [11]) may be integrated in the camera head to implement the image reconstruction.

In contrast to these approaches, the multiresolution sensor may be programmed to readout a lower resolution image at any user-defined frame rate (including video or faster) with no additional hardware (decimation and averaging occur on-chip) or software overhead. The same optics setting can be used for the varying resolutions maintaining a constant field of view such that no part of the scene needs to be discarded.

Robotics: The primary motivation for the work described in this paper was to reduce the computational complexity of algorithms devoted to autonomous navigation for vehicles in space. For power- and size-constrained missions, the multiresolution imager serves a dual purpose: navigational sensor and science sensor. In the former, for instance, low resolution data may be used for stereo vision-based autonomous navigation, while high-resolution visual data can be obtained for public relations and science.

Target Tracking: In both commercial and military applications, real-time tracking poses a difficult challenge. In a variety of defense imaging systems, for instance, high-speed target acquisition, tracking, and homing are essential operations. The multiresolution sensor can play a pivotal role in reducing the amount of image data that must be processed. For example, depending on the distance to the expected target, the sensor can be read out at the lowest resolution necessary such that the target covers a small number of pixels. Once potential targets are identified, small windows around each possible target can be read out at high resolution leading to better clutter rejection and faster processing speed. Tracking and homing can also benefit from similar optimal adjustment of resolution and windowing.

In the commercial arena, subject tracking can be used in applications such as PC videoconferencing and perimeter surveillance to reduce the required bandwidth of video transmissions. In the former, a low resolution "coarse" image is quickly read out and the subject of interest is identified. In subsequent frames, a high resolution window around the subject is read out and transmitted. Frequent repetition of this process is used to update the desired readout window. In the case of perimeter surveillance, the multiresolution capability can be exploited in a variety of ways. For example, low resolution imagery can be continually transmitted to a central processing workstation until movement or another triggering mechanism is alerted which would then signal the sensor or sensor bank to switch into high-resolution mode and start recording image data.

Biological Vision: There is a trend among some researchers today [12], [13] to mimic simple biological vision systems in silicon. The multiresolution architecture can be extended to help realize these goals. Specifically, in the case of a retina, a foveated architecture in which the center pixels are read out at high resolution while the outer pixels are readout at lower resolutions is required. In the current sensor, kernel size is limited to either square or rectangular pixels and kernels must be of uniform size in the vertical direction. It is possible to vary the kernel size in the horizontal direction. In order to mimic biological systems, programmability of kernel size in both directions in a single frame would be required but could be realized with an extension of the approach described here.

V. Summary

The multiresolution sensor, shown in Fig. 10, demonstrates the versatility of CMOS active pixel image sensors. On-chip column circuitry performs block averaging using programmable kernel sizes. The images of George Washington in Fig. 11 from a dollar bill illustrate the sensor's multiresolution ability. Shown are images at full resolution, 2 × 2, 4 × 4, and 8 × 8 kernel configurations. The accuracy of averaging is within 2% of the average calculated from full resolution image data. With power consumption as low as 5 mW and 30-Hz minimum frame rate operation for any resolution, this programmable multiresolution sensor can significantly reduce camera system complexity and power where multiresolution image processing is required, yet retain very high imaging performance of 80-dB dynamic range comparable to the very best CCD's.

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She began her professional career as a registered nurse after completing the A.S. degree. As a Ph.D. student, her work centered on the design and implementation of charge-coupled device (CCD) image sensors and on-chip image processing using charge domain circuits. In the summer of 1988, she worked for the Ford Aerospace and Communications Corporation and designed the linear CCD image sensor flown on the Mars Observer Mission. Following completion of the Ph.D. degree, she joined the NASA Jet Propulsion Laboratory (JPL) in 1991, as a Member of the Technical Staff in the Microdevices Technology Section. At JPL she designed concurrent processing ASIC's including neural networks and a high-speed SIMD path planner integrated circuit. She was a key member of the APS R&D Team and was one of the three original inventors of the APS technology. She managed several tasks at JPL and served as Study Team Leader on two studies related to imaging systems and on-board data processing. In 1995, she left JPL to form Photobit, La Crescenta, CA, and serves as CEO. She has published more than 25 technical papers and holds two patents with several patents pending.

While an undergraduate at Columbia, Dr. Kemeny received the Helen Rubenstein Outstanding Women of Science Scholarship Award. Her high-speed SIMD path planner integrated circuit was nominated by JPL for an R&D 100 Award. In 1994, she received the JPL Exceptional Service Award for Concurrent Processor Development, a Group Achievement Award for Concurrent Processor Development, and a Group Achievement Award for the STRVIB Payload Development Team. In 1996, she received the NASA Group Achievement Award for her contributions to the JPL CMOS APS research effort.

Roger Panicacci earned the B.S. degree in electrical engineering from the University of California, Berkeley, in 1985 and the M.S.E.E. degree from the University of California, Santa Barbara, in 1989.

He is both a Senior Engineer and an original founder of Photobit, La Crescenta, CA. He is responsible for VLSI circuit design and layout, test, and integration of Photobit APS products. At Photobit, he completed the design of 576 × 432 element sensor with on-chip ADC that was 100% successful on first silicon. Prior to Photobit, he was with the Jet Propulsion Laboratory's Advanced Imager Technology Group where his responsibilities included imager chip architecture, digital control logic, analog circuitry, and board level test system. He has been the primary designer on several APS chips including a multiresolution robotics imaging APS, a very high frame rate APS for NRL, and JPL's 1024 × 1024 element sensor with on-chip analog to digital conversion. Prior to JPL, he was with Kodak Berkeley Research for four years in their VLSI design group where he was responsible for the design of a number of macrocells (FIFO's, ROM's, PLA's I/O cells), a mixed analog-digital 1-GHz optical sensor chip for a high-speed optical tape drive, a number of board-level designs for communication applications, and the design of a data block decoder/error corrector for the Kodak PhotoCD product. Prior to Kodak, he was with Delco System Operations for four years as a VLSI Design Engineer.

In 1996, Mr. Panicacci received the NASA Group Achievement Award for his contributions to the JPL CMOS APS research effort.

Bedabrata Pain received the Bachelor of Technology degree in 1986 from the Indian Institute of Technology, Kharagpur, India, and the Masters and Ph.D. degrees in electrical engineering at Columbia University, NY, in 1989 and 1993, respectively.

In 1993, he joined the Jet Propulsion Laboratory (JPL) as a Post-Doctoral Research Associate. Since 1994, he has been a Member of the Technical Staff at JPL. Currently, he heads the advanced imager and focal-plane technology group at JPL and is involved in research and development of CMOS active pixel sensors, infrared sensors, and integrated charged particle detectors. His current research interests include low-noise, low-power mixed analog/digital VLSI, and integrated sensor technology.

Dr. Pain is the recipient of two NASA achievement awards for his contribution to the active pixel sensor technology and the airborne visible/infrared imaging spectrometer.

Larry Matthies received the Ph.D. degree in computer science from Carnegie Mellon University, Pittsburgh, PA, in 1989.

He is now a Member of the Technical Staff at the Jet Propulsion Laboratory (JPL) in Pasadena, CA. His research to date has focused on 3-D sensing and representation methods for autonomous navigation. In particular, he has applied stochastic modeling and recursive estimation methods to 3-D shape and motion estimation from stereo vision, from image sequences, and from the combination of stereo vision and sonar. At JPL, he has developed a real-time stereo vision system for range estimation in cross-country navigation. His research interests include sensing, world modeling, and planning for robotics and related applications. He has also worked and taught in the field of computer graphics at the National Research Council of Canada, the Tektronix Corporation, and the University of Waterloo.

Eric R. Fossum (S'80–M'84–SM'91) received the B.S. degree in physics (with Honors) and engineering from Trinity College, Hartford, CT, in 1979, the M.S. degree in applied physics in 1980 from Yale University, New Haven, CT, and the Ph.D. degree from Yale in electrical engineering in 1984.

During the summers of 1981–1983, he was with the Hughes Aircraft Company, Canoga Park, CA, working on various problems related to infrared focal-plane array detector and readout structures. He joined Columbia University in 1984 as an Assistant Professor and was engaged primarily in research on silicon charged-coupled devices (CCD's) for on-focal-plane image processing and III–V CCD's for very high speed signal processing. Other activities included novel devices and structures for fiber-based optical interconnects and the low energy ion beam modification of semiconductor surfaces. He was promoted to Associate Professor in 1989. He joined the Jet Propulsion Laboratory (JPL) in 1990 as a Technical Assistant Section Manager. At JPL he was responsible for developing visible and infrared imaging technology and programs in a section of approximately 110 researchers and engineers. He initiated and led JPL's pioneering research in CMOS active pixel image sensors. In 1995, he helped to found Photobit, La Crescenta, CA, and in 1996, joined Photobit as Chief Scientist. At Photobit, he is responsible for advanced research and development of CMOS active pixel sensors for commercial, industrial, government, and consumer applications. He also serves as Chairman of the Board. In 1996, he was appointed as an Adjunct Professor of Electrical Engineering at the University of California, Los Angeles (UCLA). He will teach classes in image sensors at UCLA as well as work with graduate students while remaining at Photobit. His area of expertise is in semiconductor devices physics and device microfabrication with specialization in charge-coupled devices (CCD's), active pixel sensors (APS), and infrared focal-plane technology.

Dr. Fossum has held an IBM Graduate Fellowship and the Howard Hughes Doctoral Fellowship. In 1994, he was also appointed as a JPL Senior Research Scientist in recognition of his research contributions. In 1996, his CMOS APS team received the NASA Group Achievement Award. He has received several prestigious awards including the Yale Becton Prize in 1984, the IBM Faculty Development Award in 1984, the National Science Foundation Presidential Young Investigator Award in 1986, the JPL Lew Allen Award for Excellence in 1992, and the NASA Exceptional Achievement Medal in 1996. He has organized and chaired many conferences. He founded the biannual IEEE Workshop on CCD's and Advanced Image Sensors and the SPIE biannual conference on Infrared Readout Electronics. He has published more than 170 technical papers and holds nine U.S. patents, with another 12 patents pending. He has served on several IEEE and SPIE conference committees and is a member of the SPIE. He is presently the Guest Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES special issue on solid-state image sensors to be published in October 1997 and an Associate Editor for IEEE TRANSACTIONS ON VLSI SYSTEMS.